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[CRITICAL AREA COMPUTATION OF COMPOSITE FAULT MECHANISMS USING VORONOI DIAGRAMS]

Abstract

Disclosed is a method that determines critical areas associated with different types of fault mechanisms in an integrated circuit design. The invention does this by constructing individual Voronoi diagrams for critical areas of individual fault mechanisms and a composite Voronoi diagram based on the individual Voronoi diagrams. The invention computes the critical area for composite fault mechanisms of the integrated circuit design based on the composite Voronoi diagram.